REMARKS

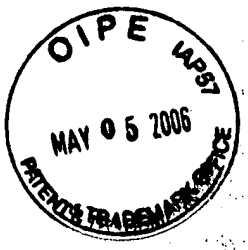
Claims 1-61 are pending in this application, of which claims 1, 8 and 32 are in independent form. The Examiner has acknowledged that claims 2-7 and 9-25 would be allowable if rewritten in independent form. Favorable reconsideration is requested in view of the following remarks.

Raymond Szeto, a colleague of the undersigned, and I have spoke with Examiner Kim of the USPTO (on January 19, 2006) regarding the rejected to claims. Discussed was claim 1 and how that claim distinguished over the cited art. Specifically discussed was the Beckwith failure to disclose an out-of-order microinstruction pointer.

The Examiner rejected Claims 1, 8, and 26-38 under 35 U.S.C. §102(b) as being anticipated by Beckwith et al., U.S. Patent No. 5,136,696.

Claim 1, as amended, calls for ... a plurality of the pointers associated with a common macroinstruction... Support for this claim amendment is found on page 5, line 3 through page 7, line 16. Claim 1 is distinct over Beckwith. Claim 1 now calls for "...an out-of-order microinstruction pointer (μIP) stack for storing pointers in a microcode (μcode) execution core, a plurality of the pointers associated with a common macroinstruction, the plurality of pointers placed on the out-of order microinstruction pointer stack and removed from the microinstruction pointer stack before it is known if a sequence of microinstructions pointed to by the plurality of pointers is valid."

Beckwith neither describes nor suggests an out-of-order microinstruction pointer (μIP) stack. Even though Beckwith pushes microinstructions onto a stack, a common practice in processor design to handle branch operations, for a set of microinstructions associated with a common macroinstruction, these microinstructions are not sequenced out-of-order. "The microinstructions of the instruction interpreter are sequenced in the same manner as a normal instruction sequence." (Beckwith, col. 8, lines 23-25). Therefore, for a common macroinstruction, Beckwith only suggests an ordered microinstruction pointer stack. The ordered microinstruction pointer stack does not take microinstructions out-of-order or remove



pointers from the microinstruction pointer stack "before it is known if a sequence of microinstructions pointed to by the pointers is valid."

Claims 8 and 26-38 are allowable either because they depend either from claim 8 or from claim 32, both of which contain analogous limitations as claim 1.

The Examiner objected Claims 2-7 and 9-25 because they depend upon a rejected base claim. Claims 1 and 8 have been amended and are allowable for reasons discussed above. Claims 2-7 and 9-25 are allowable at least for the reasons discussed in their respective base claims.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a **$450** check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 5/2/06

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